HCTL-2001-A00

Quadrature Decoder/Counter Interface ICs

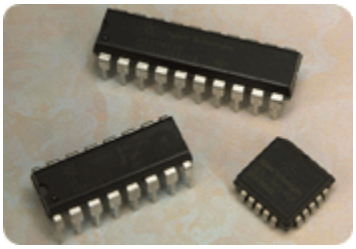
Description

HCTL-2xxx series is a direct drop-in replacement for HCTL-2000, HCTL-2020 and HCTL-2016 which has been obsoleted. It is a CMOS IC that performs quadrature decoding, bus interfacing and counter functions.

HCTL-2xxx series is designed to improve system performance in digital, closed loop motion control systems and digital data input systems. The highlight of our ICs are it being enhanced to lead-free (RoHs compliant) and customers can easily upgrade their existing HCTL decoders with this direct drop-in. Also, with the use of Schmitt-triggered CMOS input and input noise filter, it allows a more reliable operation in a noisy environment. This product is suitable for machine control manufacturers such as servo motors applications.

Lead (PB) Free
RoHS 6 fully compliant

Lifecycle status: Active



Request customization of this product

Features

- Interfaces Encoder to Microprocessor
- 14Mhz Clock Operation
- High Noise Immunity: Schmitt Trigger inputs and digital Noise filter
- 16-Bit Binary Up/Down counter
- Latched output
- 8-Bit Tristate interface
- 8,12 or 16-Bits operating modes
- Quadrature Decoder Output Signals, Up/Down and count
- Cascade output Signals, Up/Down and Count
- Substantially Reduced System Software
- 5V Operation (Vdd-Vss)
- TTL/CMOS Compatible I/O
- Operating Temperature : -40^{o}C to 85^{o}C
- 16-Pin PDIP, 20-Pin PDIP, 20-Pin PLCC

Applications

- Test and Measurement Equipment

- Safety Equipment
- Servo and stepper motors
- Printers
- Fax Machines and Photo Copiers
- Home Appliances
- Meters and Monitoring
- White Goods and Appliances

Benefits

- Provides flexibility in choice of output data
- This decoder will help to reduce the processing power to release the microprocessor load in decoding the encoder signal. Thus, it allows the processor to increase its capacity and run at faster speed.
- No external hardware (counter) is required
- Capabile of filtering all external encoder signal noise
- Provides design flexibility. PLCC packages need less space on system boards
- Lead-Free (RoHs compliant)

HCTL-2001-A00, HCTL-2017-A00 / PLC, HCTL-2021-A00 / PLC

Quadrature Decoder/Counter Interface ICs

Data Sheet

Description

The HCTL-2xx1(7)-A00/PLC is CMOS ICs that performs the quadrature decoder, counter, and bus interface function. The HCTL-2xx1(7)-A00/PLC is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The HCTL-2xx1(7)-A00/PLC consists of a quadrature decoder logic, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2001-A00 contains 12-bit counter and HCTL-2017-A00/PLC or HCTL-2021-A00/PLC contains 16-bit counter and provides TLL/CMOS compatible tri-state output buffers. Operation is specified for a temperature range from –40 to +85°C at clock frequencies up to 14MHz.

The HCTL-2021-A00/PLC provides quadrature decoder output signals and cascade signals for use with many standard computer ICs.

Features

- Interfaces Encoder to Microprocessor
- 14 MHz Clock Operation
- High Noise Immunity:
- Schmitt Trigger Inputs and Digital Noise Filter
- 16-Bit Binary Up/Down Counter
- Latched Outputs
- 8-Bit Tristate Interface
- 8, 12 or 16-Bit Operating Modes
- Quadrature Decoder Output Signals, Up/Down and Count
- Cascade Output Signals, Up/Down and Count
- Substantially Reduced System Software
- 5V Operation ($V_{DD} – V_{SS}$)
- TTL/CMOS Compatible I/O
- Operating Temperature: -40°C to 85°C
- 16-Pin PDIP, 20-Pin PDIP, 20-Pin PLCC

Applications

- Interface Quadrature Incremental Encoders to Microprocessors
- Interface Digital Potentiometers to Digital Data Input Buses

Part Number	Description	Pinout	Package
HCTL-2001-A00	14 MHz clock operation. 12-bit counter.	PINOUT A	PACKAGE A
HCTL-2017-A00	14 MHz clock operation. 16-bit counter.	PINOUT A	PACKAGE A
HCTL-2017-PLC	14 MHz clock operation. 16-bit counter.	PINOUT C	PACKAGE C
HCTL-2021-A00	14 MHz clock operation. 16-bit counter. Quadrature decoder output signals. Cascade output signals.	PINOUT B	PACKAGE B
HCTL-2021-PLC	14 MHz clock operation. 16-bit counter. Quadrature decoder output signals. Cascade output signals.	PINOUT D	PACKAGE C

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_{IN}	-0.3 to (VDD +0.3)	V
Storage Temperature	T_S	-55 to +150	C
Operating Temperature [1]	T_A	-40 to +85	C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	4.5 to 5.5	V
Ambient Temperature [1]	T_A	-40 to +85	C

Table 3. DC Characteristics V_{DD} = 5V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL [2]	Low-Level Input Voltage				1.5	V
VIH [2]	High-Level Input Voltage		3.5			V
VT+	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
VT-	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
VH	Schmitt-Trigger Hysteresis		1.0	2.0		V
IIN	Input Current	VIN=VSS or VDD	-10	1	+10	µA
VOH [2]	High-Level Output Voltage	IOH = -3.75 mA	2.4	4.5		V
VOL [2]	Low-Level Output Voltage	IOL = +3.75mA		0.2	0.4	V
IOZ	High-Z Output Leakage Current	VO=VSS or VDD	-10	1	+10	µA
IDD	Quiescent Supply Current	VIN=Vss or VDD		1	100	µA
CIN [3]	Input Capacitance	Any Input		5		pF
COUT [3]	Output Capacitance	Any Output		5		pF

Notes:

1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5V to +5.5V), $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.7V_{DD}$; typical values are $V_{OH} = V_{DD} - 0.5V$ and $V_{OL} = V_{SS} + 0.2V$
3. Including package capacitance

Switching Characteristics

Table 5. Switching Characteristics Max/Min specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to +85 ^{0}C, C_L = 40 pf

Symbol	Description		Min.	Max.	Units
1	tCLK	Clock Period	70		ns
2	tCHH	Pulse width, clock high	28		ns
3	tCD	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	tODE	Delay time, OE fall to valid data		65	ns
5	tODZ	Delay time, OE rise to Hi-Z state on D0-7		40	ns
6	tSDV	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	tCLH	Pulse width, clock low	28		ns
8	tSS	Setup time, SEL before clock fall	20		ns
9	tOS	Setup time, OEN before clock fall	20		ns
10	tSH	Hold time, SEL after clock fall	0		ns
11	tOH	Hold time, OE after clock fall	0		ns
12	tRST	Pulse width, RST low	28		ns
13	tDCD	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	tDSD	Hold time, last data byte stable after next SEL state change	10		ns
15	tDOD	Hold time, data byte stable after OE rise	10		ns
16	tUDD	Delay time, U/D valid after clock rise		45	ns
17	tCHD	Delay time, CNTDCDR or CNTCAS high after clock rise		45	ns
18	tCLD	Delay time, CNTDCDRor CNTCAS low after clock fall		45	ns
19	tUDH	Hold time, U/D stable after clock rise	10		ns
20	tUDCS	Setup time, U/D valid before CNTDCDR or CNTCAS rise	tCLK-45		ns
21	tUDCH	Hold time, U/D stable after CNTDCDR or CNTCAS rise	tCLK-45		ns

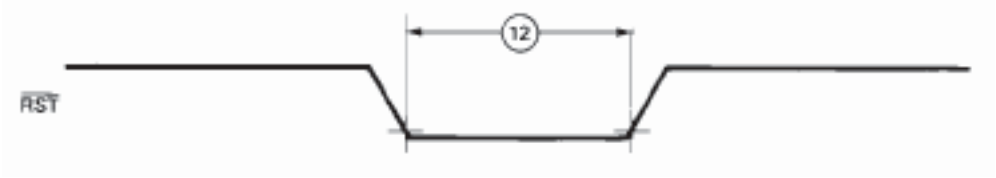


Figure 1. Reset Waveform

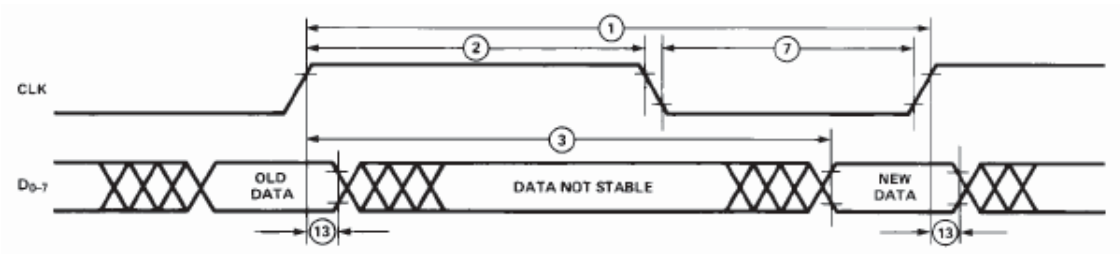
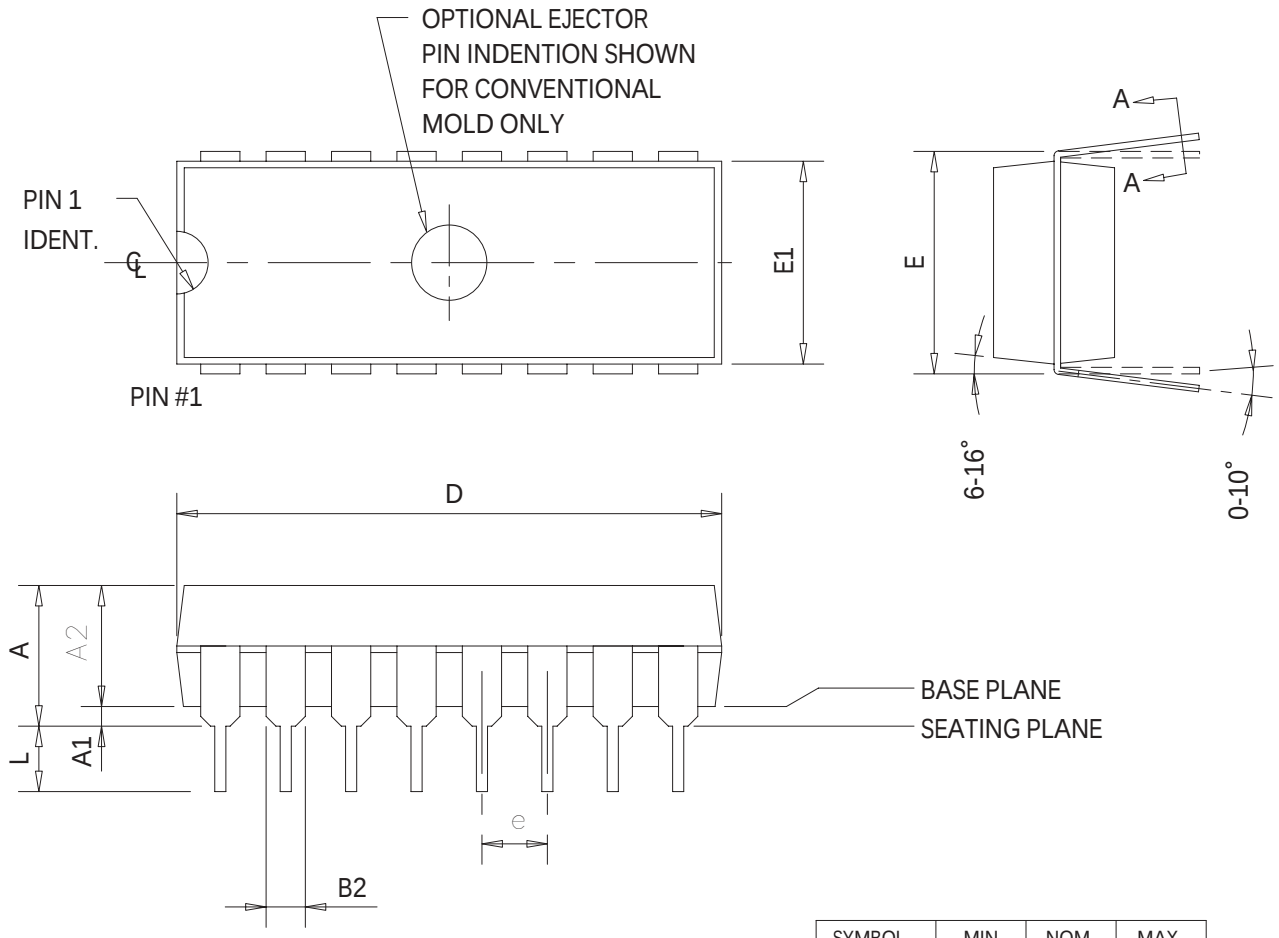


Figure 2: Waveforms for Positive Clock Edge Related Delays

APPENDIX A

PACKAGE A



SYMBOL	MIN.	NOM.	MAX.
A	-	-	.175
A1	0.015	-	-
A2	0.115	0.130	0.195
B	0.014	-	0.022
B1	0.014	0.018	0.020
B2	0.550	0.600	0.650
C	0.008	-	0.014
C1	0.008	0.010	0.012
D	0.740	0.750	0.760
E	0.295	0.310	0.325
E1	0.240	0.250	0.260
e	0.100 BSC.		
L	0.125	-	0.150

ALL DIMENSIONS ARE IN INCHES